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Design issues for edge nodes in agile all-photonic networks

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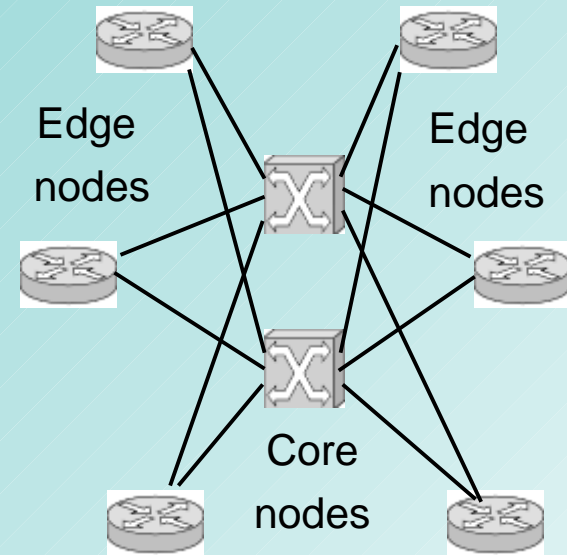
Agenda

- I. Overview of an agile all-photonic network
- II. Functionality of the Edge Node
- III. Control and signalling
- IV. Proposed implementation of the Edge Node
- V. Implementation requirements
- VI. Implementation issues and limitations
- VII. Implementation options: comparison
- VIII. Edge Node emulation results (software model)
- IX. Ongoing work : downscaled models of the AAPN

I. Overview of an agile all-photonic network (AAPN)

AAPN:

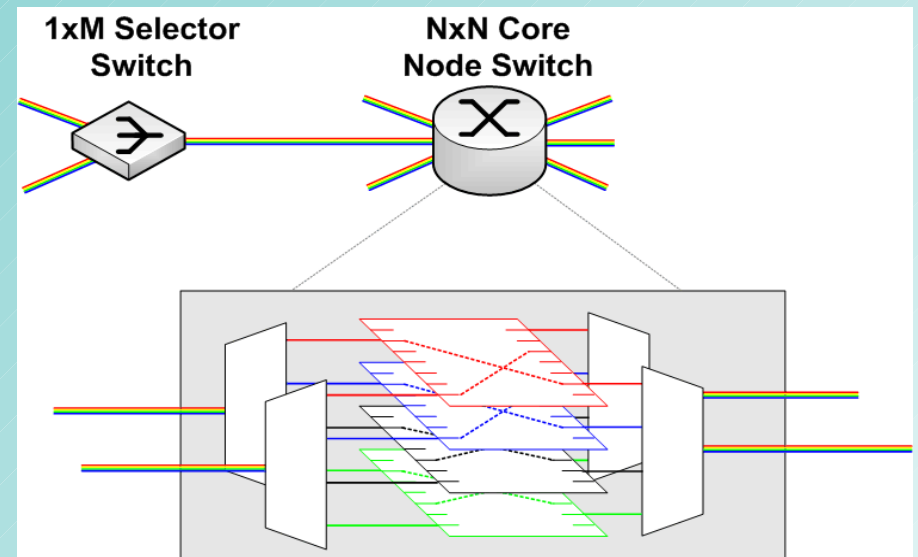
- wavelength division multiplexed network
- consists of several overlaid stars
- stars are formed by **edge nodes** interconnected by optical **core nodes**
- core nodes perform fast switching of lightpaths
- data is transmitted in fixed-size slots:
10 μ s (100kb in 10Gb/s link)



I. Overview of an agile all-photonic network (AAPN)

Core Node:

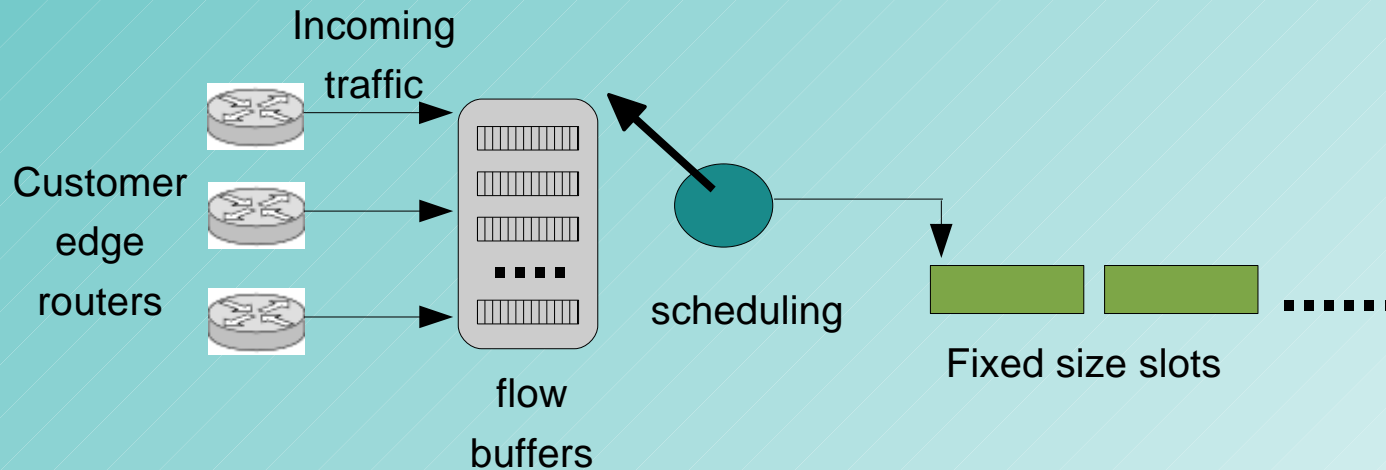
- fully optical and bufferless
- stack of space switches, one for each wavelength
- establishes light paths between edge node pairs
- dynamically configures to adapt to the traffic demands (as reported by the edge nodes)
- can reconfigure very fast (target: $1\mu\text{s}$)
- time interval between reconfigurations:
1 slot to ∞



II. Functionality of the Edge Node

Main functionality of the Edge Node

- hybrid electro-optical device
- access point for customer edge routers
- aggregates incoming traffic into fixed size slots organized by flow (source-destination pair)
- it sends traffic information to the core node for reconfiguration



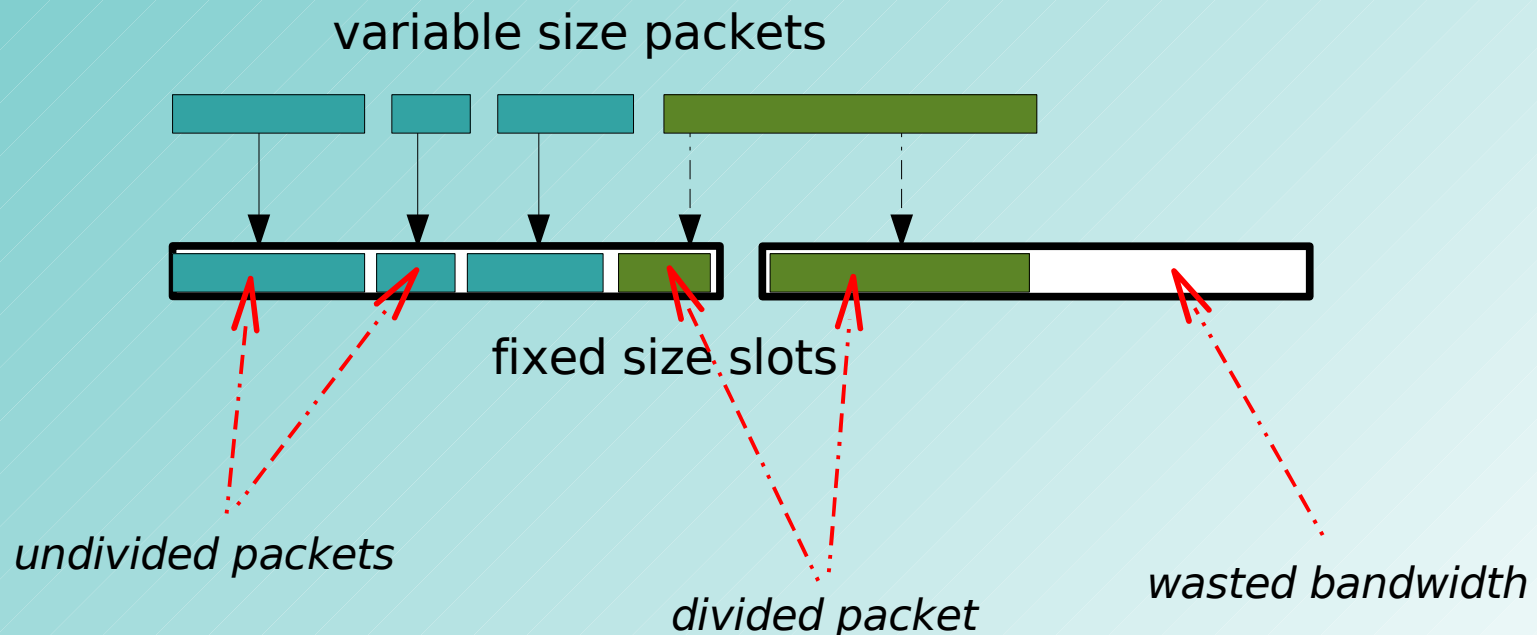
Additional functionality of the Edge Node

Edge nodes maintain a look-up table with **N-1** edge nodes (network with **N** edge nodes) and customer sub networks addresses (MPLS labels) assigned to them.

Subnetwork	Edge Node ID
137.122.*	11
120.23.*	14
156.220.*	15

II. Functionality of the Edge Node (slot assembly and traffic aggregation)

- single slot consists only of packets with identical source and destination
- a packet may be divided to fill a slot exactly; the rest of the packet will then be at the beginning of the next slot of the same flow
- a *time-out* is used in the slot aggregation process: a slot may be left with some empty space when the traffic load is low



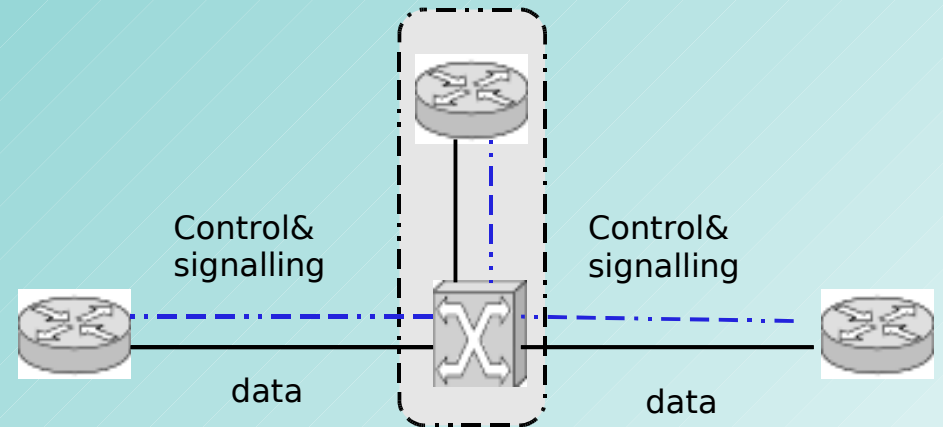
III. Signalling and controlling

Signalling:

- *out-of-band* signalling requires a separate wavelength
- *in-band* signalling utilizes the same wavelength as the transmitted data

Control information:

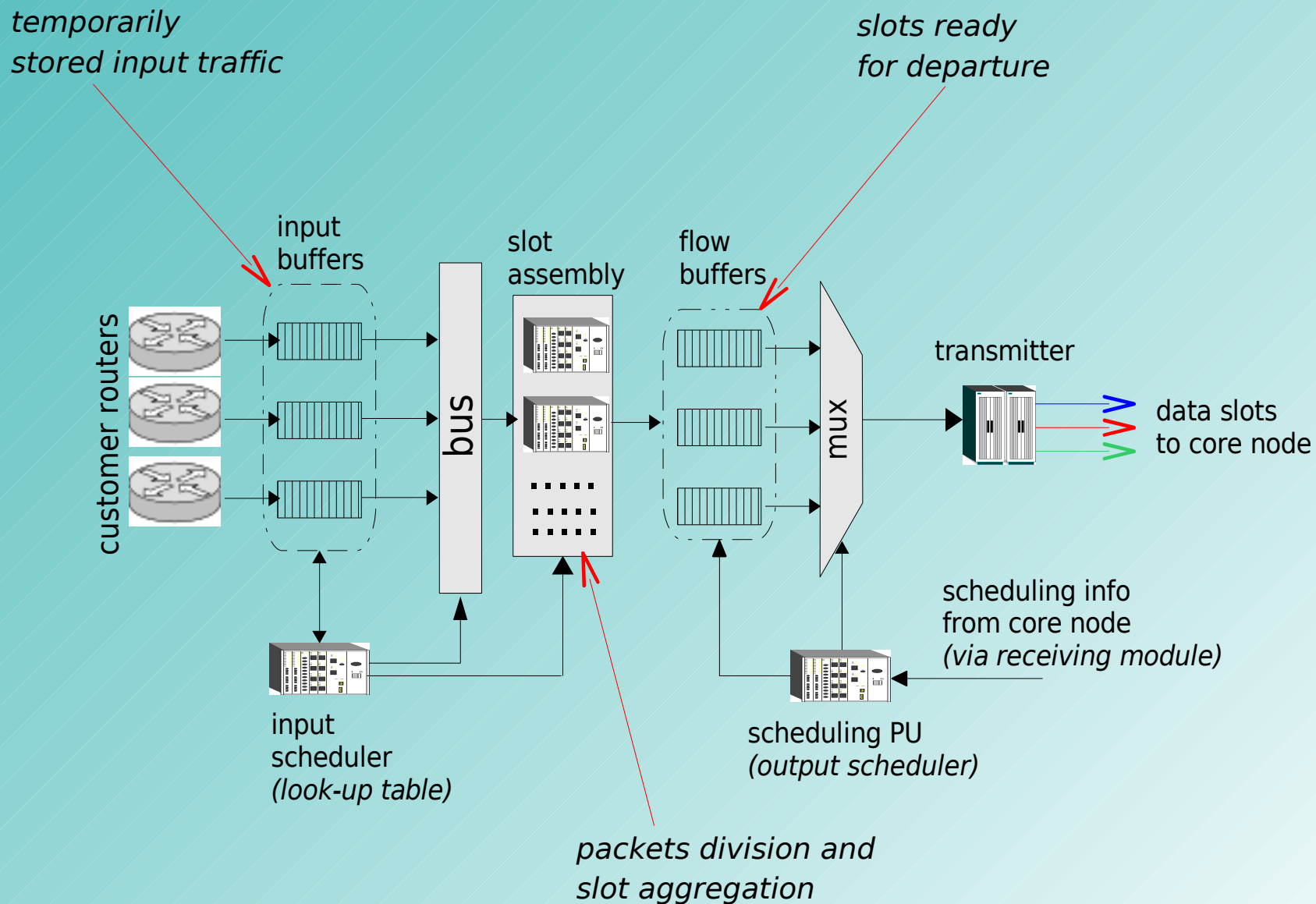
- can be transmitted in separate slots of the same size, called “control slots”
- could be sent inside the data slots



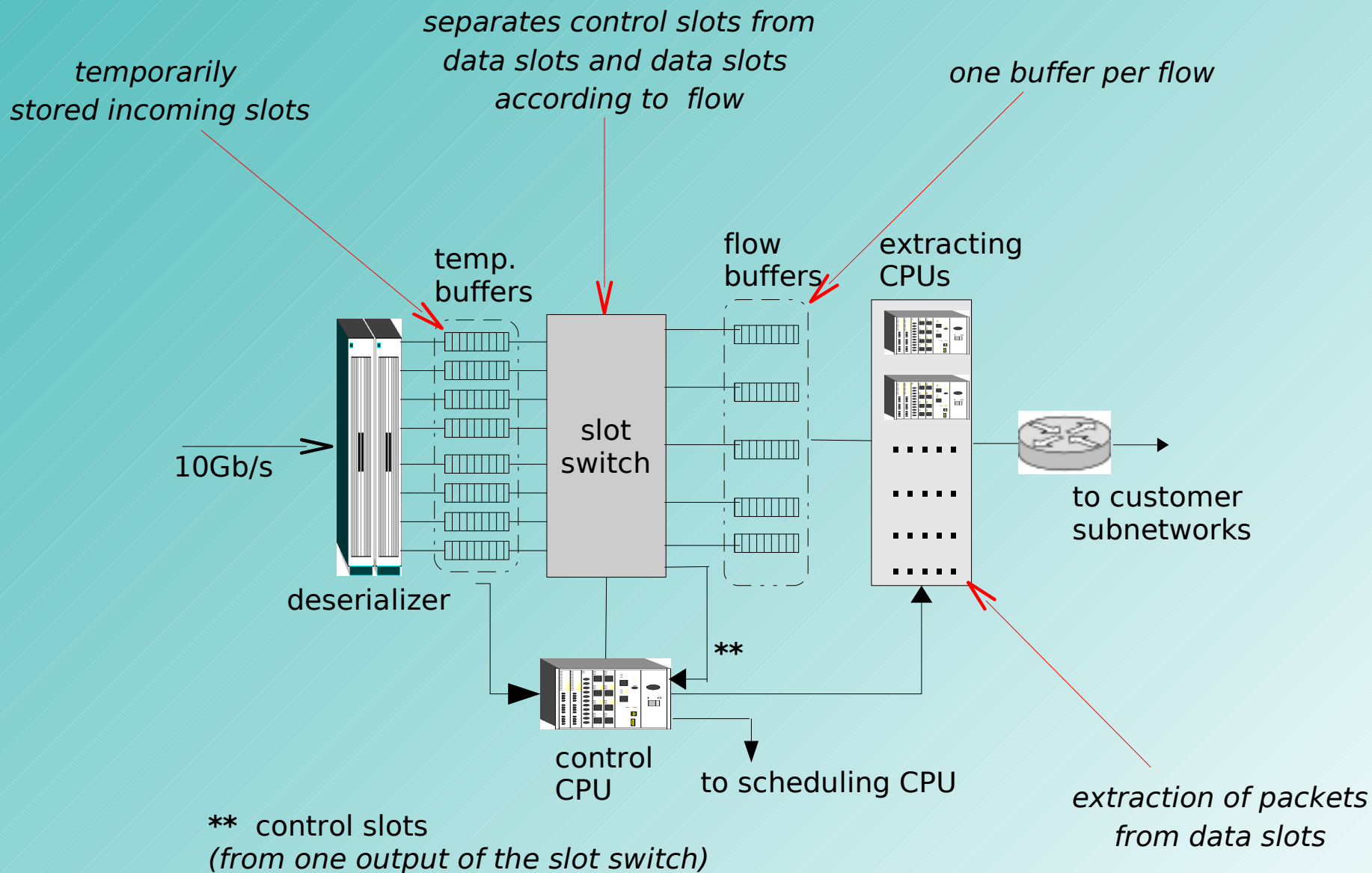
Controlling the core node:

- one of the edge nodes is collocated with the core node and it plays role of controller

IV. Proposed implementation of the Edge Node: Transmitting Module



IV. Proposed implementation of the Edge Node: Receiving Module



V. Implementation Requirements

- Mass production components that are commercially available right now
- The maintenance cost (opex) should be low, even if the entry costs of purchase and first installation (capex) are high
- Bottlenecks in internal communication between devices should be removed or decreased as much as possible
- The architecture should be vendor-independent
- Compatibility with common standards to ensure that programming tasks can be done using regular software tools

VI. Implementation issues and limitations

- Memory speed
 - What memory should we use ?
 - DDR3 works with 1.3 Gb/s / 1.3GHz
 - What memory controller should we use?
 - ATI R600 GDDR4 handles 2.6GHz DDR4
 - Opteron embedded controller handles 25Gb/s
- Internal data transmission bottleneck (local bus)
 - PCI64-133MHz handles ~8.5Gb/s
 - PCI64-166MHz will soon handle ~10.5Gb/s
- Scalability
- Synchronisation between R&W from buffers

VII. Implementation options: comparison

Model:	HARDWARE	SOFTWARE	HYBRID
Implementation:	<p>Custom designed board with FPGAs</p> <p>Embedded fast memory (DDR-2/3 or QDR-II)</p>	<p>Mass production multi-cpu board with 64bit CPUs</p> <p>Standard memory (DDR-2/3)</p>	<p>Mass production multi-cpu board with extension FPGA cards</p>
Pro:	<p>Low power consumption</p> <p>Efficient hardware resources utilisation</p> <p>High level of integration</p>	<p>Low cost of implementation and maintenance</p> <p>Easy to upgrade and modify</p> <p>Dynamic load balance between CPUs</p>	<p>Bypass internal bottlenecks</p> <p>Division of tasks between main CPUs and FPGAs</p>
Con:	<p>Scalability issues</p> <p>High cost of first design and prototype</p> <p>High cost of upgrades</p>	<p>Requires vendor specific compiler for efficient hardware utilisation</p> <p>Issues with internal data transfer</p>	<p>Issues with compatibility</p>

VIII. Edge Node emulation results

(software model + Pentium IV 2.8GHz)

To estimate the capabilities of low-cost mass production CPUs as the processing units in the Edge Node

Benchmark that measures the maximum speed for writing and reading sequences of bytes from multiple buffers in the RAM:

Buffers: 64 x 300kB

Reading: 10Gb/s

Writing: 2.8 Gb/s

Software implementation of the scheduler that emulates traffic aggregation and slot assembling in the Edge Node:

Full load: 1.2Gb/s

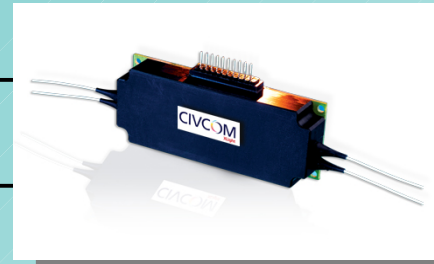
2 tasks: 2.1Gb/s

IX. Ongoing work : downscaled models of the AAPN

*Hardware model with
Altera development boards*

Speed: ~100Mb/s

*One of the edge nodes is
the controller.*



Edge nodes

Core node



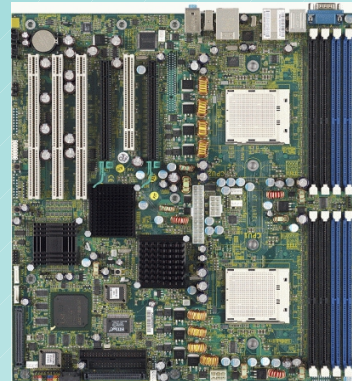
Edge nodes

ctrl

Software model with multi-CPU

64bit mother board

Speed: ~1Gb/s

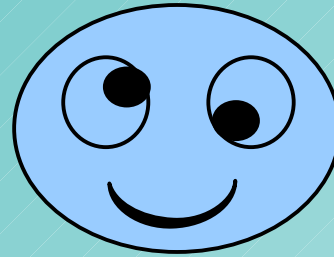


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gigabit NICs



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Thank You !



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