SoC Packet Switch With Reconfigurable Bandwidth - H/W Demonstrator

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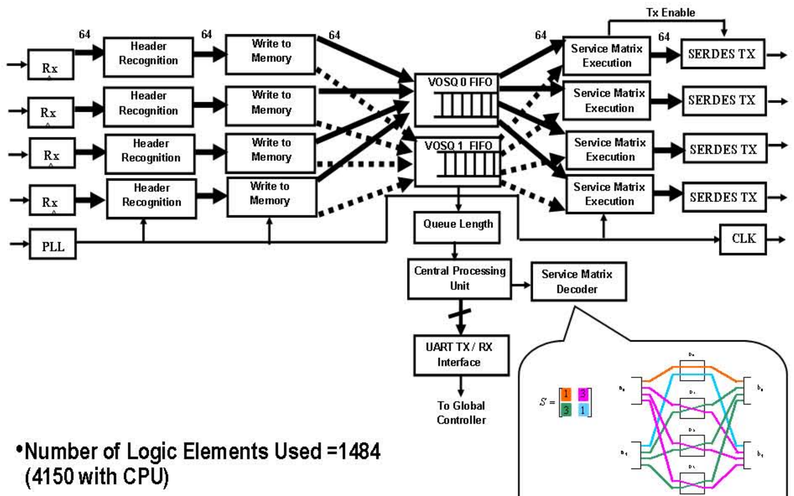
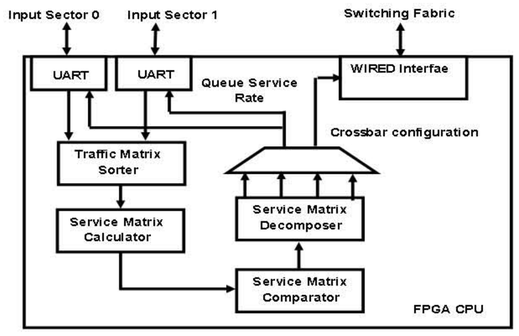
Input Sector (Common Memory Switch)



- Number of Logic Elements Used =1484 (4150 with CPU)
- FIFO Depth is 128 words and the width is 64 bits

Global Controller



- Responsible for computing the service matrix for each Input Sector and the crossbar configuration
- Number of Logic Elements Used = 4205
- Implemented within the FPGA processor core

Research Interactions

Industry:

Funding from:

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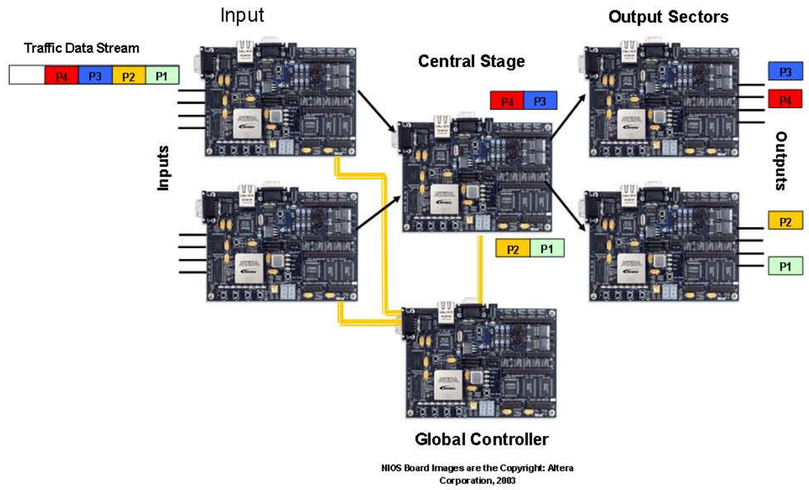
Advantages Of Our Packet Switch Architecture

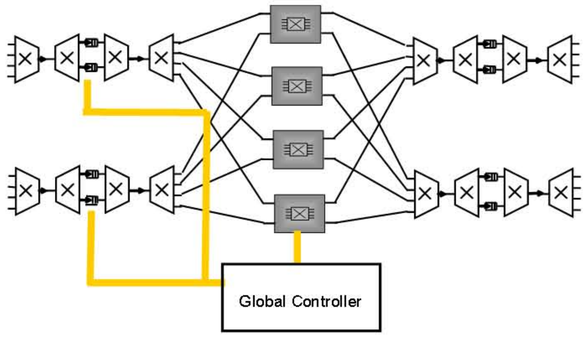
1. Scalability – the advantages of this architecture are more evident for large number of ports and sectors.
2. Configuration of central stage on a per-packet basis is NOT necessary
3. Delay performance is close to that of the Output Queued Switch (the 'ideal' architecture)
4. Central stage does most of the transporting – optics is better suited for this; whereas, the Sectors do most of the switching – electronics is better suited for this.
5. Decrease in power dissipation by using an optical crossbar and / or Flexible Bandwidth Provision scheduler

Packet Switch Demonstrator

Hardware View:

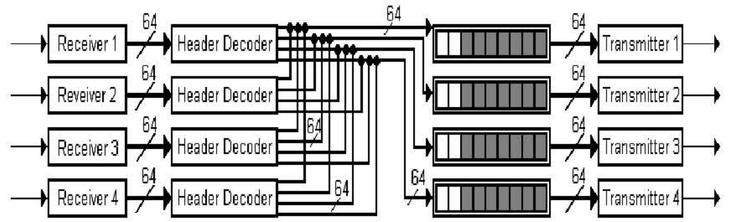


Logical View:



- Port line rate for the demonstrator is 10 Mbps. Design is scalable up to 2.5 Gbps provided the use of Stratix GX FPGA Devices.
- Packet size is 64 bits for this prototype

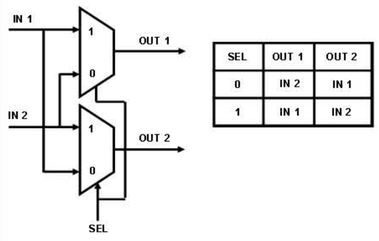
Output Sector (Common Memory Switch)



- Number of Logic Elements Used = 1417
- Queues are all dedicated output queues

Reconfigurable Central stage

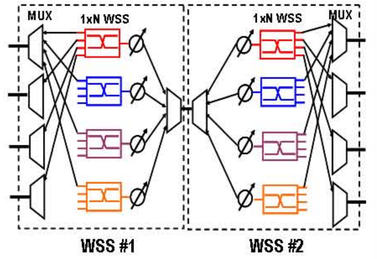
Current: Electrical



SEL	OUT 1	OUT 2
0	IN 2	IN 1
1	IN 1	IN 2

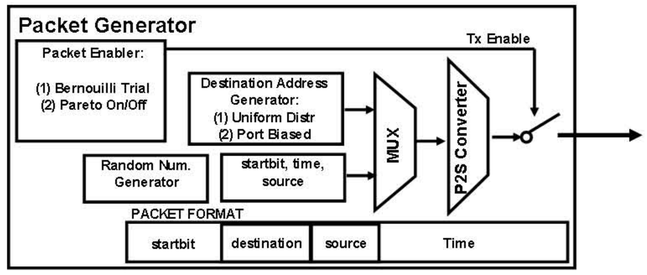
2 x 2 Digital Switch Using 9 FPGA Logical Elements

Target: Optical



2x2 Stackup Using Optical Wavelength Selective Switches (by Metconnex)

Traffic Generator and Traffic Analyzer



- Traffic Analyzer is implemented using the NIOS processor on a FPGA and connects to the Traffic Generator and to the output of the packet switch
- Data Produced from Traffic Analyzer Per Port:
  - total # of packets, packet delay vs time, & histogram of packet delays
- Total Number of Logic Elements Consumed for an 8 port Packet Generator is 3872 and uses 113664 MEs.